WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a dielectric pedestal located above and integral to a substrate and having first sidewalls;

a channel region located above said dielectric pedestal and having second sidewalls; and

source and drain regions opposing said channel region and each substantially spanning one of said second sidewalls.

2. The semiconductor device as recited in Claim 1 wherein said first and second sidewalls are substantially coincident.

3. The semiconductor device as recited in Claim 1 wherein each of said source and drain regions further substantially spans one of said first sidewalls.

4. The semiconductor device as recited in Claim 1 wherein said dielectric pedestal and said substrate comprise at least a portion of a silicon-on-insulator (SOI) substrate.

5. The semiconductor device as recited in Claim 1 wherein said channel region, said dielectric pedestal and said substrate comprise at least a portion of a silicon-on-insulator (SOI) substrate.

6. The semiconductor device as recited in Claim 1 wherein said dielectric pedestal is at least a portion of a buried oxide (BOX) layer located in said substrate.

7. The semiconductor device as recited in Claim 1 further comprising a silicide layer over at least portions of said source and drain regions.

8. The semiconductor device as recited in Claim 1 further comprising a gate structure including a gate oxide located above said channel region and a gate electrode located above said gate oxide.

9. The semiconductor device as recited in Claim 8 wherein said gate oxide has a thickness ranging between about 0.2 nm and about 2 nm.

10. The semiconductor device as recited in Claim 1 wherein said channel region has a length ranging between about 2 nm and about 100 nm.

11. The semiconductor device as recited in Claim 1 wherein said channel region has a thickness ranging between about 1 nm and about 20 nm.

12. A method of manufacturing a semiconductor device, comprising:

providing a substrate having a channel layer located over a buried dielectric layer;

forming a gate structure over said channel layer;

removing portions of said channel layer and said buried dielectric layer using at least a portion of said gate structure as a mask, thereby defining a dielectric pedestal having first sidewalls and a channel region having second sidewalls; and

forming source and drain regions opposing said channel region and each substantially spanning one of said second sidewalls.

13. The method as recited in Claim 12 wherein said first and second sidewalls are substantially coincident.

14. The method as recited in Claim 12 wherein each of said source and drain regions further substantially spans one of said first sidewalls.

15. The method as recited in Claim 12 wherein said providing a substrate includes providing a silicon-on-insulator (SOI) substrate.

16. The method as recited in Claim 12 further comprising forming a silicide layer over at least portions of said source and drain regions.

17. The method as recited in Claim 16 wherein said forming said silicide layer includes forming spacers opposing said gate structure and partially extending over said source and drain regions and employing said spacers as a mask.

18. The method as recited in Claim 12 wherein said forming said gate structure includes forming a gate oxide above said channel region and forming a gate electrode above said gate oxide.

19. The method as recited in Claim 18 wherein said gate oxide has a thickness ranging between about 0.2 nm and about 2 nm.

20. The method as recited in Claim 12 wherein said channel region has a length ranging between about 2 nm and about 100 nm.

21. The method as recited in Claim 12 wherein said channel region has a thickness ranging between about 1 nm and about 20 nm.

22. The method as recited in Claim 12 further comprising forming spacers on opposing sides of said gate structure, wherein said mask includes said spacers.

23. The method as recited in Claim 12 wherein said removing includes etching through said channel layer and at least partially into said buried dielectric layer.

24. The method as recited in Claim 12 wherein said forming said source and drain regions includes depositing one selected from the group consisting of:

silicon;

silicon-germanium; and

polysilicon.

25. The method as recited in Claim 24 wherein said forming said source and drain regions includes doping said one.

26. An integrated circuit device, comprising:

a semiconductor device, including:

a dielectric pedestal located above and integral to a substrate and having first sidewalls;

a channel region located above said dielectric pedestal and having second sidewalls; and

source and drain regions opposing said channel region and each substantially spanning one of said second sidewalls;

an interlevel dielectric layer located over said semiconductor device; and

vias spanning said interlevel dielectric layer and contacting said source and drain regions.

27. The integrated circuit device as recited in Claim 26 wherein said first and second sidewalls are substantially coincident.

28. The integrated circuit device as recited in Claim 26 wherein each of said source and drain regions further substantially spans one of said first sidewalls.

29. The integrated circuit device as recited in Claim 26 wherein said dielectric pedestal and said substrate form at least a portion of a silicon-on-insulator (SOI) substrate.

30. The integrated circuit device as recited in Claim 26 wherein said channel region, said dielectric pedestal and said substrate form at least a portion of a silicon-on-insulator (SOI) substrate.

31. The integrated circuit device as recited in Claim 26 wherein said dielectric pedestal is at least a portion of a buried oxide (BOX) layer located in said substrate.

32. The integrated circuit device as recited in Claim 26 wherein said semiconductor device includes a silicide layer over at least portions of said source and drain regions.

33. The integrated circuit device as recited in Claim 26 wherein said semiconductor device includes a gate structure having a gate oxide located above said channel region and a gate electrode located above said gate oxide.

34. The integrated circuit device as recited in Claim 33 wherein said gate oxide has a thickness ranging between about 0.2 nm and about 2 nm.

35. The integrated circuit device as recited in Claim 26 wherein said channel region has a length ranging between about 2 nm and about 100 nm.

36. The integrated circuit device as recited in Claim 26 wherein said channel region has a thickness ranging between about 1 nm and about 20 nm.